24. The field effect transistor of Claim 21, wherein the second silicide portion comprises nickel silicide.

REMARKS

This Amendment is in response to the Office Action mailed March 30, 2000. Claims 1-20 are pending, and Claims 1-17 have been withdrawn as being directed to a non-elected invention, and Claims 18-20 have been rejected.

By this amendment, non-elected Claims 1-17 have been cancelled from this application, Claim 18 has been amended to correct an inadvertent typographical error, and has further been amended to more clearly distinguish the claimed invention from the art of record. New Claims 21-24 have been added. No new matter has been added. In view of the amendments above and remarks below, Applicant respectfully requests reconsideration and further examination.

Overview of the Invention

A MOSFET includes a double silicided source/drain structure wherein the source/drain terminals include a silicided source/drain extension, a deep silicided source/drain region, and a doped semiconductor portion that surrounds a portion of the source/drain structure such that the silicides are isolated from the MOSFET body node. In a further aspect of the present invention, a barrier layer is formed around a gate electrode to prevent electrical shorts between a silicided source/drain extension and the gate electrode. A deep source/drain is then formed, self-aligned to sidewall spacers that are formed subsequent to the silicidation of the source/drain extension.

Objections

The Examiner has objected to an informality in Claim 18, and has required correction. More particularly, the Examiner points out that in Claim 18, line 7, "second implanted regions" should read "second implanted region".

By this amendment, Claim 18 has been amended as suggested by the Examiner to correct this typographical error. This amendment is not intended to alter the scope of Claim 18, and has not been made in view of any art-based rejection.

Rejections under 35 USC § 102

Claims 18-20 have been rejected under 35 USC § 102(e) as being anticipated by Kimura (U.S. Patent No. 5,883,418). The Examiner indicates that Kimura discloses a semiconductor device with a silicide structure and that Kimura more particularly teaches a gate electrode (5) having sidewalls (9), a silicidation barrier (26) adjacent the sidewalls (9), a silicide layer (15b) adjacent to the gate electrode (5), a pair of source/drain terminals (6) self-aligned to the gate electrode (5), wherein the source/drain terminals (6) comprise a first implanted region (7a), a second silicide layer (16a), second implanted regions (14a) and a third silicide layer (16b). The Examiner also indicates that Kimura teaches a second silicide layer (16a) contained within the first implanted region (7a). With regard to Claim 20 the Examiner indicates that Kimura teaches silicide layers (40,41) being thicker than each of silicide layers (16a, 16b).

Applicant has carefully reviewed Kimura and believes that Kimura shows transistors which have only a single silicide layer in each of the source/drain regions. Kimura does not disclose a structure as set forth in the amended Claims.

Claim 18 has been amended to make clear that **each of** the source/drain terminals comprise a first implanted region, a second silicide layer; a second implanted region and a third silicide layer. In the invention defined by the amended Claims, a gate electrode has one source/drain terminal disposed on

each of two sides, and each of those source/drain terminals includes two silicide layers. One silicide layer in each source/drain terminal is disposed in the implanted source/drain extension region, and another, thicker, silicide layer in each source/drain terminal is disposed in the deep S/D implant region.

In view of the amendments and remarks above, Applicant respectfully submits that the rejections under 35 USC § 102 second paragraph have been overcome. Furthermore, Kimura does not appear to suggest nor provide motivation for the invention as defined by the amended Claims.

New Claims 21-24

New Claims 21-24 have been added and are directed to a field effect transistor embodying the present invention. Support for these Claims can be found in the specification from page 8, line27, to page 10, line 26; and in Figs. 2-7.

Conclusion

It is respectfully submitted that the pending Claims 18-24 are in condition for allowance and such action is earnestly solicited.

Correspondence in this matter should continue to the address of record.

If a telephone conversation with Applicant's undersigned representative would in any way facilitate the examination and passage to issue of this application, then please contact the undersigned at telephone number (503) 264-1421.

Respectfully submitted,

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